

In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown. Please cancel claims 2, 12 and 23 without prejudice.

- 1 1. (Currently Amended) A computer system comprising:
  - 2 a bus; and
  - 3 a chipset, coupled to the bus, having:
    - 4 a slew rate detection mechanism to detect a slew rate of a signal
    - 5 transmitted from the chipset over the bus and to generate a signal indicating a
    - 6 status of the slew rate; and
    - 7 control logic, coupled to the slew rate detection mechanism, to receive the
    - 8 signal and to adjust the slew rate based upon the state of the signal.
    - 9 ~~to detect the slew rate of a signal transmitted over the bus via the chipset, and to~~
    - 10 ~~adjust the slew rate based upon the state of the signal.~~
  - 1 2. (Cancelled)
  - 1 3. (Original) The computer system of claim 1 wherein the chipset further comprises an input/output (I/O) buffer coupled to the control logic.
  - 1 4. (Currently Amended) The computer system of claim 1 ~~2~~ wherein the control logic reduces the slew rate if the signal received from the slew rate detection mechanism indicates that the slew rate is too fast.

1 5. (Currently Amended) The computer system of claim 1 2 wherein the control logic  
2 increases the slew rate if the signal received from the slew rate detection mechanism  
3 indicates that the slew rate is too slow.

1 6. (Currently Amended) The computer system of claim 1 2 wherein the slew rate  
2 detection mechanism includes a capacitor, coupled to the bus, to integrate the received  
3 signal current.

1 7. (Original) The computer system of claim 6 wherein the slew rate detection  
2 mechanism further includes:  
3 a reference current generator to generate a reference current; and  
4 a comparator to compare the received signal current to the reference current.

1 8. (Original) The computer system of claim 7 wherein the slew rate detection  
2 mechanism further includes:  
3 a first converter, coupled to the capacitor and the comparator to convert the signal  
4 current to a signal voltage; and  
5 a second converter, coupled to the reference current generator and the comparator  
6 to convert the reference to a reference voltage.

1 9. (Original) The computer system of claim 6 wherein the comparator is an  
2 operational amplifier.

1 10. (Original) The computer system of claim 1 wherein the bus is a high-speed  
2 bus.

1 11. (Currently Amended) A computer system comprising:

2 a main memory device;

3 a memory bus coupled to the main memory device; and

4 a memory controller, coupled to the bus, having:

5 a slew rate detection mechanism to detect a slew rate of a signal

6 transmitted from the memory controller over the bus and to generate a signal

7 indicating a status of the slew rate; and

8 control logic, coupled to the slew rate detection mechanism, to receive the

9 signal and to adjust the slew rate based upon the state of the signal.

10 ~~to detect the slew rate of a signal transmitted over the bus via the chipset, and to~~

11 ~~adjust the slew rate based upon the state of the signal.~~

1 12. (Cancelled)

1 13. (Currently Amended) The computer system of claim ~~11 12~~ wherein the control

2 logic reduces the slew rate if the signal received from the slew rate detection mechanism

3 indicates that the slew rate is too fast.

1 14. (Currently Amended) The computer system of claim ~~11 12~~ wherein the control

2 logic increases the slew rate if the signal received from the slew rate detection

3 mechanism indicates that the slew rate is too slow.

1 15. (Currently Amended) The computer system of claim 11 ~~12~~ wherein the slew rate  
2 detection mechanism includes a capacitor, coupled to the bus, to integrate the received  
3 signal current.

1 16. (Original) The computer system of claim 15 wherein the slew rate detection  
2 mechanism further includes:

3 a reference current generator to generate a reference current; and  
4 a comparator to compare the received signal current to the reference current.

1 17. (Original) The computer system of claim 16 wherein the slew rate detection  
2 mechanism further includes:

3 a first converter, coupled to the capacitor and the comparator to convert the signal  
4 current to a signal voltage; and  
5 a second converter, coupled to the reference current generator and the comparator  
6 to convert the reference to a reference voltage.

1 18. (Original) A method comprising:

2 transmitting a signal from an input/output (I/O) buffer within a chipset over a bus;  
3 receiving the signal at a slew rate detection mechanism within the chipset via the  
4 bus;  
5 generating a signal indicating the status of the slew rate; and  
6 adjusting the slew rate at control logic within the chipset based upon the signal.

1 19. (Original) The method of claim 18 further comprising generating a reference  
2 current at the chipset.

1 20. (Original) The method of claim 19 further comprising:  
2 converting the signal current to a signal voltage;  
3 converting the reference current to a reference voltage; and  
4 comparing the reference voltage to the signal voltage.

21. (Original) The method of claim 18 wherein adjusting the slew rate comprises  
modifying the amplification of a second signal at the I/O buffer.

22. (Currently Amended) An apparatus comprising:  
a slew rate detection mechanism to detect the slew rate of a signal transmitted  
from a memory controller over a bus via the memory controller, and to adjust the slew  
rate based upon the state of the signal; and to detect the slew rate and generate a signal to  
indicate the status of the slew rate. bus

1 23. (Cancelled)

1 24. (Currently Amended) The computer system of claim 22 23 further comprising  
2 control logic, coupled to the slew rate detection mechanism, to receive the signal and  
3 modify the slew rate based upon the signal.

1 25. (Original) The apparatus of claim 24 further comprising an input/output (I/O)  
2 buffer coupled to the control logic.

1 26. (Original) The apparatus of claim 22 wherein the slew rate detection  
2 mechanism includes a capacitor, coupled to the bus, to integrate the received signal  
3 current.

1 27. (Original) The apparatus of claim 26 wherein the slew rate detection  
2 mechanism further includes:  
3 a reference current generator to generate a reference current; and  
4 a comparator to compare the received signal current to the reference current.

1 28. (Original) The apparatus of claim 27 wherein the slew rate detection  
2 mechanism further includes:  
3 a first converter, coupled to the capacitor and the comparator to convert the signal  
4 current to a signal voltage; and  
5 a second converter, coupled to the reference current generator and the comparator  
6 to convert the reference to a reference voltage.